Comprehensive Final Exam for Computer Logic Design (CDA 3201)

Fall 2001

NAME: _____ **SSN:** _____

Welcome to the comprehensive final exam in *Computer Logic Design* (CDA 3201). You have 120 minutes. Read each problem carefully. There are twelve required problems (each worth 8 points and 4 total points for free) and one extra credit problem worth 5 points. You may have with you (on your desk, that is) a calculator, pencils, erasers, blank paper, and a lucky rabbit's foot. You are given Table 2.2 (page 91) of your text (Boolean algebra postulates and theorems) on the last page of this exam. Please start each numbered problem on a new sheet of paper and do not write on the back of the sheets. Submit everything in problem order. No sharing of calculators. Good luck and be sure to show your work!

Problem #1 (5 minutes)

Answer the following problems related to number systems

a) Convert 1234_{10} to hexadecimal.

b) Represent "negative 7" in sign magnitude, 1's complement, and 2's complement. Use the minimum number of bits possible.

Problem #2 (5 minutes)

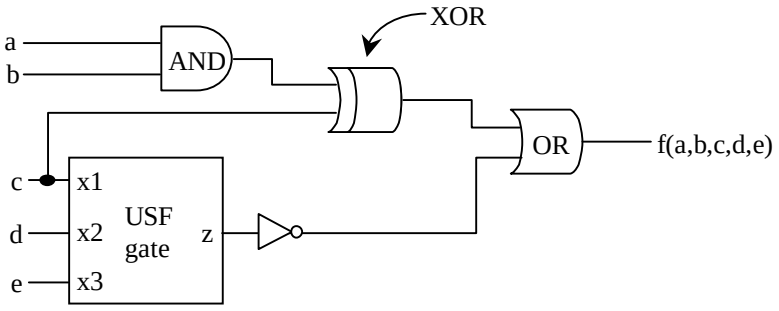
Minimize the following expression using Boolean algebra postulates and theorems. Carefully show your work in a step-by-step fashion and identify the postulate or theorem used in each step.

$$f(a,b,c) = \overline{\overline{(a+\bar{b})}\,\overline{(b \cdot c)}}$$

Problem #3 (10 minutes)

You are given the below circuit. The gate labled "USF gate" has the truth table also given below. Your job is to analyze the given circuit and come-up with a minimized two-level circuit for the same function that uses AND and OR gates (you may assume that complementary inputs, if needed, are directly available - e.g., both a and $\bar{a}$ are available). Draw the minimized two-level circuit.

x1	x2	x3	z
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



Problem #4 (10 minutes)

Minimize the following for SOP form.

$$f(a,b,c,d,e) = \bar{a} \cdot \bar{b} \cdot \bar{c} \cdot \bar{e} + a \cdot \bar{b} \cdot \bar{e} + \bar{a} \cdot \bar{b} \cdot c \cdot \bar{d} + a \cdot \bar{b} \cdot c \cdot \bar{d} \cdot e + b \cdot c \cdot d \cdot \bar{e}$$

Problem #5 (10 minutes)

Implement the truth table given below using a 3-to-8 decoder, an 8-to-1 multiplexer, and a 4-to-1 multiplexer (you should have three implementations shown in your answer). A "dc" is a don't care.

A	B	C	f
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	dc
1	0	0	1
1	0	1	1
1	1	0	dc
1	1	1	0

Problem #6 (5 minutes)

Give the truth table for a binary full-adder and then implement using any kind of basic gates (NOT, AND, OR, XOR) that you want.

Problem #7 (5 minutes)

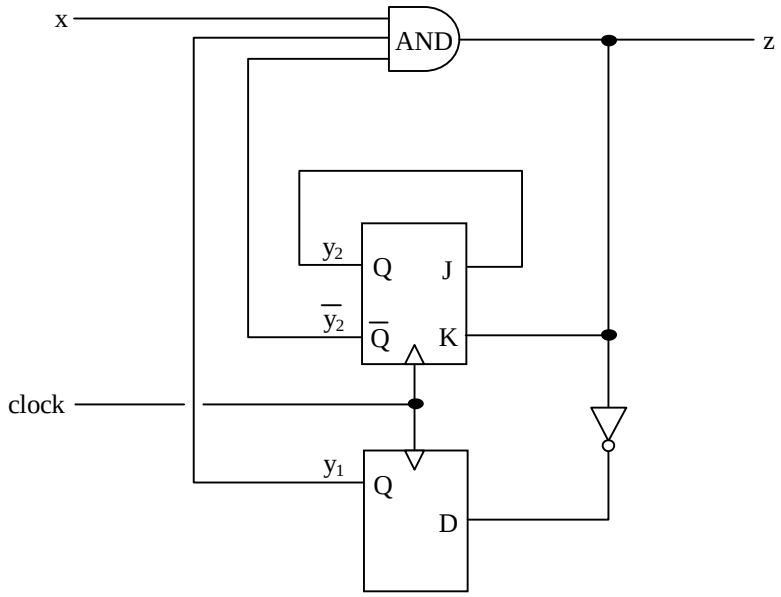
Sketch an SR NOR latch and correctly label all inputs and output. Give the next state table. Identify any illegal inputs. Show how this illegal input condition can be "fixed" (you may not simply assume that the illegal inputs will never occur).

Problem #8 (10 minutes)

Using T latches and basic gates, design a counter that counts in the following sequence, 000, 100, 010, 101, 111, and repeats the seqeunce.

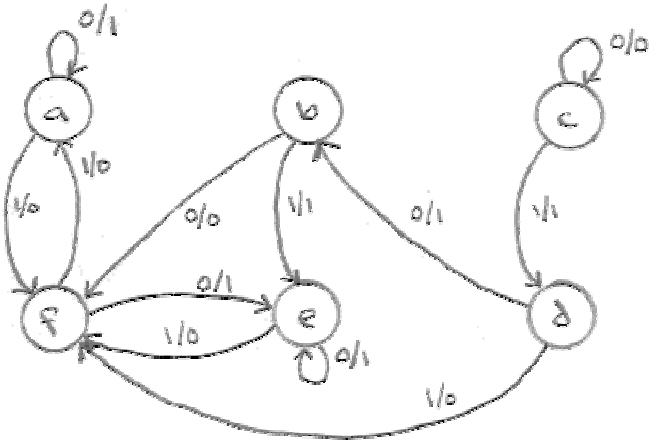
Problem #9 (15 minutes)

Analyze the following synchronous sequential circuit. You are to give the state diagram for this circuit.



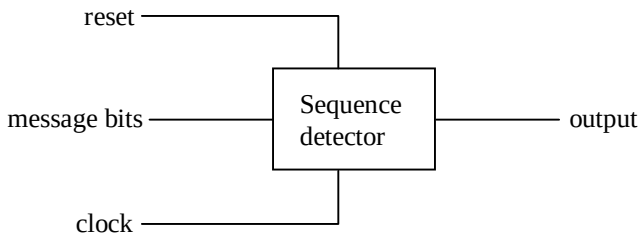
Problem #10 (20 minutes)

Given the state diagram below, design a synchronous sequential circuit using D flip-flops to implement it. Your implementation must have a minimum number of flip-flops and a "good" state assignment. Carefully show your work including the state assignment procedure. You need not draw the final circuit, simply giving the excitation equations for the D flip-flops and the output equation is sufficient.



Problem #11 (10 minutes)

Give a state diagram for a synchronous sequential ciruit to detect a start of a message sequence of 11 or 001. That is, when the circuit is reset, it outputs a 1 when the sequence 11 or 1001 is first detected. The input sequence is synchronous with a clock source. A black box view of the circuit is show below.



Problem #12 (10 minutes)

Answer the following questions about pulse-mode and fundamental-mode sequential circuits.

a) What is a pulse-mode sequential circuit? Carefully describe the attributes of such a circuit comparing it to a synchronous sequential circuit.

b) What is a fundamental-mode sequential circuit? Carefully describe the attributes of such a circuit comparing it to synchronous and pulse-mode sequential ciruits.

c) When would you use a pulse-mode or fundamental-mode sequential circuit instead of a synchronous sequential circuit? State at least two good reasons.

Extra Credit (5 minutes)

Give three practical ideas for improving the class (not including the lab in this case). For full credit, the ideas must not entail additional resources or reducing the content of the course. General complaints or rants will not help me or future students very much.

TABLE 2.2 BOOLEAN ALGEBRA POSTULATES AND THEOREMS

Expression	Dual
$P2(a): a + 0 = a$	$P2(b): a \cdot 1 = a$
$P3(a): a + b = b + a$	$P3(b): ab = ba$
$P4(a): a + (b + c) = (a + b) + c$	$P4(b): a(bc) = (ab)c$
$P5(a): a + bc = (a + b)(a + c)$	$P5(b): a(b + c) = ab + ac$
$P6(a): a + \bar{a} = 1$	$P6(b): a \cdot \bar{a} = 0$
$T1(a): a + a = a$	$T1(b): a \cdot a = a$
$T2(a): a + 1 = 1$	$T2(b): a \cdot 0 = 0$
$T3: \quad \bar{\bar{a}} = a$	
$T4(a): a + ab = a$	$T4(b): a(a + b) = a$
$T5(a): a + \bar{a}b = a + b$	$T5(b): a(\bar{a} + b) = ab$
$T6(a): ab + a\bar{b} = a$	$T6(b): (a + b)(a + \bar{b}) = a$
$T7(a): ab + a\bar{b}c = ab + ac$	$T7(b): (a + b)(a + \bar{b} + c) = (a + b)(a + c)$
$T8(a): \overline{a + b} = \bar{a}\bar{b}$	$T8(b): \overline{ab} = \bar{a} + \bar{b}$
$T9(a): ab + \bar{a}c + bc = ab + \bar{a}c$	$T9(b): (a + b)(\bar{a} + c)(b + c) = (a + b)(\bar{a} + c)$
$T10(a): f(x_1, x_2, \ldots, x_n) = x_1 f(1, x_2, \ldots, x_n) + \bar{x}_1 f(0, x_2, \ldots, x_n)$	
$T10(b): f(x_1, x_2, \ldots, x_n) = [x_1 + f(0, x_2, \ldots, x_n)][\bar{x}_1 + f(1, x_2, \ldots, x_n)]$	